WHAT IS CLAIMED IS:

1. A memory controller comprising a serial/parallel converter section for converting serial input data into parallel data, an FIFO memory section for temporarily storing converted data, a memory section connected to the FIFO memory section to store data for a frame and a second FIFO memory section for temporarily storing the data read out from the frame memory section.

2. A memory controller according to claim 1, wherein said memory section can be accessed continuously in synchronism with the system clock according to said input data.

3. A memory controller according to claim 1, wherein the data bit width of said memory section is made equal to n times of the bit width of said input data and data for a number of frames up to as many as (n-2) times of the number of input pixels can be read out of said memory section for said input data while the frequency of accessing said memory section can be reduced to a half or less than a half of the video signal input frequency.

4. A memory controller according to claim 1, wherein the size of said FIFO memory is minimized by

selecting a continuous write period for writing data into said memory section, taking the time period required for a command necessary for said memory section.

5. A memory controller according to claim 1, wherein the data bit width of said memory section is made equal to n times of the bit width of said input data and the frequency of accessing said memory section is reduced to less than the video signal input frequency.

6. A memory controller comprising a serial/parallel converter section for performing a serial/parallel conversion of converting a-bit (a being a positive integer) input data into axn-bit data, an FIFO memory section for temporarily storing converted axn-bit data, a memory section connected to the FIFO memory section to store data for a frame and a second FIFO memory section for temporarily storing the axn-bit data read out from the frame memory section.

7. A memory controller according to claim 6, further comprising a video signal output controlling section for receiving the output of said second FIFO memory section and converting them into output video signals according to instructions from the output side.

8. A memory controller according to claim 1, wherein the data bit width of said memory section is made equal to 2n times of the bit width of said input data and data for a number of frames up to as many as (2n-2) times of the number of input pixels can be read out of said memory section for said input data while the frequency of accessing said memory section can be reduced to a half or less than a half of the video signal input frequency.

9. A memory controller according to claim 3, wherein the bit width of said input data is equal to 8 bits and said n is equal to 3, whereas said data bit width of said memory section is equal to 24.

10. A memory controller according to claim 3, wherein the bit width of said input data is equal to 8 bits and said n is equal to 4, whereas said data bit width of said memory section is equal to 32.

11. A memory controller according to claim 1, wherein said memory section comprises a plurality of memory units.

Sub A1

12. A liquid crystal display apparatus comprising:

an interface for transforming various video

signals and transmission signals standard video signals;

a decoder for transforming standard video signals into video signals for displaying images on liquid crystal;

a liquid crystal display panel; and

a drive section for driving said display panel according to said video signals,

characterized in that

said decoder includes a memory controller comprising a serial/parallel converter section for converting serial input data into parallel data, an FIFO memory section for temporarily storing converted data, a memory section connected to the FIFO memory section to store data for a frame and a second FIFO memory section for temporarily storing the data read out from the frame memory section.

ADD B1

Add D1